WHAT IS CLAIMED IS:

1. A power-on detector comprising:

a reference potential generation circuit which generates a reference potential; and

a first comparator which compares a first voltage generated on the basis of the reference potential output from the reference potential generation circuit and a potential of a first potential supply source, and a second voltage generated on the basis of the reference potential and a potential of a second potential supply source different from the potential of the first potential supply source,

wherein power-on is detected when a potential difference between the potentials of the first and second potential supply sources upon power-on becomes larger than a sum of the first and second voltages.

2. The detector according to claim 1, wherein the reference potential generation circuit includes a band gap reference circuit.

3. The detector according to claim 2, wherein the band gap reference circuit comprises a first circuit unit which is so constituted as to generate a first current having a positive temperature characteristic, a second circuit unit which is so constituted as to generate a second current having a negative temperature characteristic, and a third circuit unit which is so constituted as to add the first current output from the

first circuit unit and the second current output from the second circuit unit and generate the reference potential on the basis of the added current.

4. The detector according to claim 3, wherein the first circuit unit comprises a second comparator, a first MOS transistor of a first conductivity type which has one end of a current path connected to the second potential supply source, the other end of the current path connected to a non-inverting input terminal of the second comparator, and a gate connected to an output terminal of the second comparator, a second MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source, the other end of the current path connected to an inverting input terminal of the second comparator, and a gate connected to the output terminal of the second comparator, a first resistor which has one terminal connected to said other end of the current path of the first MOS transistor, a first diode which has an anode connected to the other terminal of the first resistor and a cathode connected to the first potential supply source, and a second diode which has an anode connected to said other end of the current path of the second MOS transistor and a cathode connected to the first potential supply source, and the first circuit unit obtains an output signal from the output terminal of the second comparator.

5. The detector according to claim 4, wherein the second circuit unit comprises a third comparator, a third MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source and the other end of the current path connected to an inverting input terminal of the third comparator and receives at a gate the output signal from the first circuit unit, a fourth MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source, the other end of the current path connected to a non-inverting input terminal of the third comparator, and a gate connected to an output terminal of the third comparator, a third diode which has an anode connected to said other end of the current path of the third MOS transistor and a cathode connected to the first potential supply source, and a second resistor which has one terminal connected to said other end of the current path of the fourth MOS transistor and the other terminal connected to the first potential supply source, and the second circuit unit obtains an output signal from the output terminal of the third comparator.

6. The detector according to claim 5, wherein the third circuit unit comprises a fifth MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply

source and receives at a gate the output signal from the first circuit unit, a sixth MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source and the other end of the current path connected to said other end of the current path of the fifth MOS transistor and receives at a gate the output signal from the second circuit unit, and a third resistor which has one terminal connected to said other end of each of the current paths of the fifth and sixth MOS transistors and the other terminal connected to the first potential supply source, and the third circuit unit outputs the reference potential from a connection node between said other end of each of the current paths of the fifth and sixth MOS transistors and said one terminal of the third resistor.

7. The detector according to claim 1, further comprising a first load element which is connected between an output terminal of the reference potential generation circuit and the first potential supply source and generates the first voltage.

8. The detector according to claim 7, which further comprises a current mirror circuit that has a first current path connected to the output terminal of the reference potential generation circuit and a second current path connected to the second potential supply source via a second load element, and in which the

first comparator compares a voltage across the first load element and a voltage across the second load element.

9. The detector according to claim 8, wherein the current mirror circuit comprises a seventh MOS transistor of a second conductivity type which has one end of a current path and a gate connected to an output terminal of the reference potential generation circuit and the other end of the current path connected to the first potential supply source, and an eighth MOS transistor of the second conductivity type which has one end of a current path connected to the second load element, the other end of the current path connected to the first potential supply source, and a gate commonly connected to the gate of the seventh MOS transistor.

10. The detector according to claim 1, wherein the first comparator comprises a ninth MOS transistor of a first conductivity type which has a gate connected to an inverting input terminal, a 10th MOS transistor of the first conductivity type which has one end of a current path commonly connected to one end of a current path of the ninth MOS transistor and a gate connected to a non-inverting input terminal, a 11th MOS transistor of the first conductivity type which has one end of a current path connected to said one end of each of the current paths of the ninth and 10th MOS transistors and the other end of the current path

connected to the second potential supply source, a 12th MOS transistor of a second conductivity type which has one end of a current path and a gate connected to the other end of the current path of the ninth MOS transistor and the other end of the current path connected to the first potential supply source, a 13th MOS transistor of the second conductivity type which has one end of a current path connected to the other end of the current path of the 10th MOS transistor, the other end of the current path connected to the first potential supply source, and a gate commonly connected to the gate of the 12th MOS transistor, a 14th MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source, the other end of the current path connected to the output terminal, and a gate commonly connected to a gate of the 11th MOS transistor, and a 15th MOS transistor of the second conductivity type which has one end of a current path connected to the output terminal, the other end of the current path connected to the first potential supply source, and a gate connected to a connection node between the current paths of the 10th and 13th MOS transistors.

11. A power-on reset circuit comprising:

a data holding circuit which holds data;

a reference potential generation circuit which generates a reference potential;

a first comparator which compares a first voltage generated on the basis of the reference potential output from the reference potential generation circuit and a potential of a first potential supply source, and a second voltage generated on the basis of the reference potential and a potential of a second potential supply source different from the potential of the first potential supply source; and

a reset circuit which resets data held by the data holding circuit on the basis of an output signal from the first comparator,

wherein the reset circuit resets data held by the data holding circuit when a potential difference between the potentials of the first and second potential supply sources upon power-on becomes larger than a sum of the first and second voltages.

12. The circuit according to claim 11, wherein the data holding circuit includes at least one of a register and a latch circuit.

13. The circuit according to claim 11, wherein the reference potential generation circuit includes a band gap reference circuit.

14. The circuit according to claim 13, wherein the band gap reference circuit comprises a first circuit unit which is so constituted as to generate a first current having a positive temperature characteristic, a second circuit unit which is so constituted as to

generate a second current having a negative temperature characteristic, and a third circuit unit which is so constituted as to add the first current output from the first circuit unit and the second current output from the second circuit unit and generate the reference potential on the basis of the added current.

15. The circuit according to claim 14, wherein the first circuit unit comprises a second comparator, a first MOS transistor of a first conductivity type which has one end of a current path connected to the second potential supply source, the other end of the current path connected to a non-inverting input terminal of the second comparator, and a gate connected to an output terminal of the second comparator, a second MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source, the other end of the current path connected to an inverting input terminal of the second comparator, and a gate connected to the output terminal of the second comparator, a first resistor which has one terminal connected to said other end of the current path of the first MOS transistor, a first diode which has an anode connected to the other terminal of the first resistor and a cathode connected to the first potential supply source, and a second diode which has an anode connected to said other end of the current path of the second MOS transistor and a cathode

connected to the first potential supply source, and the first circuit unit obtains an output signal from the output terminal of the second comparator.

16. The circuit according to claim 15, wherein the second circuit unit comprises a third comparator, a third MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source and the other end of the current path connected to an inverting input terminal of the third comparator and receives at a gate the output signal from the first circuit unit, a fourth MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source, the other end of the current path connected to a non-inverting input terminal of the third comparator, and a gate connected to an output terminal of the third comparator, a third diode which has an anode connected to said other end of the current path of the third MOS transistor and a cathode connected to the first potential supply source, and a second resistor which has one terminal connected to said other end of the current path of the fourth MOS transistor and the other terminal connected to the first potential supply source, and the second circuit unit obtains an output signal from the output terminal of the third comparator.

17. The circuit according to claim 16, wherein

the third circuit unit comprises a fifth MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source and receives at a gate the output signal from the first circuit unit, a sixth MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source and the other end of the current path connected to said other end of the current path of the fifth MOS transistor and receives at a gate the output signal from the second circuit unit, and a third resistor which has one terminal connected to said other end of each of the current paths of the fifth and sixth MOS transistors and the other terminal connected to the first potential supply source, and the third circuit unit outputs the reference potential from a connection node between said other end of each of the current paths of the fifth and sixth MOS transistors and said one terminal of the third resistor.

18. The circuit according to claim 11, further comprising a first load element which is connected between an output terminal of the reference potential generation circuit and the first potential supply source and generates the first voltage.

19. The circuit according to claim 18, which further comprises a current mirror circuit that has a first current path connected to the output terminal

of the reference potential generation circuit and a second current path connected to the second potential supply source via a second load element, and in which the first comparator compares a voltage across the first load element and a voltage across the second load element.

20. The circuit according to claim 19, wherein the current mirror circuit comprises a seventh MOS transistor of a second conductivity type which has one end of a current path and a gate connected to an output terminal of the reference potential generation circuit and the other end of the current path connected to the first potential supply source, and an eighth MOS transistor of the second conductivity type which has one end of a current path connected to the second load element, the other end of the current path connected to the first potential supply source, and a gate commonly connected to the gate of the seventh MOS transistor.

21. The circuit according to claim 11, wherein the first comparator comprises a ninth MOS transistor of a first conductivity type which has a gate connected to an inverting input terminal, a 10th MOS transistor of the first conductivity type which has one end of a current path commonly connected to said one end of a current path of the ninth MOS transistor and a gate connected to a non-inverting input terminal, a 11th MOS transistor of the first conductivity type which has one

end of a current path connected to one end of each of the current paths of the ninth and 10th MOS transistors and the other end of the current path connected to the second potential supply source, a 12th MOS transistor of a second conductivity type which has one end of a current path and a gate connected to the other end of the current path of the ninth MOS transistor and the other end of the current path connected to the first potential supply source, a 13th MOS transistor of the second conductivity type which has one end of a current path connected to the other end of the current path of the 10th MOS transistor, the other end of the current path connected to the first potential supply source, and a gate commonly connected to the gate of the 12th MOS transistor, a 14th MOS transistor of the first conductivity type which has one end of a current path connected to the second potential supply source, the other end of the current path connected to the output terminal, and a gate commonly connected to a gate of the 11th MOS transistor, and a 15th MOS transistor of the second conductivity type which has one end of a current path connected to the output terminal, the other end of the current path connected to the first potential supply source, and a gate connected to a connection node between the current paths of the 10th and 13th MOS transistors.